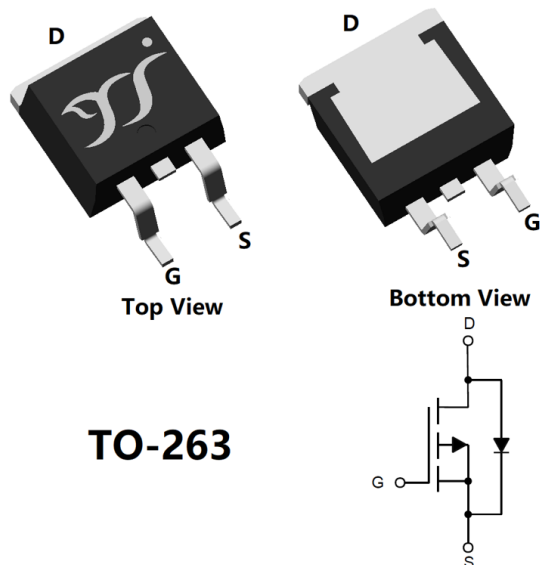


P-Channel Enhancement Mode Field Effect Transistor



TO-263

Product Summary

- V_{DS} -60 V
- I_D -100 A
- $R_{DS(ON)}$ (at $V_{GS}=-10V$) <8.8m Ω
- $R_{DS(ON)}$ (at $V_{GS}=-6V$) <10m Ω
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- Excellent stability and uniformity
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power management
- Portable equipment

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-60	V
Gate-source Voltage		V_{GS}	± 18	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	-14	A
	$T_A=100^\circ\text{C}$		-9	
	$T_C=25^\circ\text{C}$		-100	
	$T_C=100^\circ\text{C}$		-63	
Pulsed Drain Current ^A		I_{DM}	-320	A
Avalanche energy ^B		EAS	625	mJ
Total Power Dissipation ^C	$T_A=25^\circ\text{C}$	P_D	2.7	W
	$T_A=100^\circ\text{C}$		1.1	
	$T_C=25^\circ\text{C}$		178	
	$T_C=100^\circ\text{C}$		71	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	$R_{\theta JA}$	35	45	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.6	0.7	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJB100GP06H	F2	YJB100GP06H	800	/	8000	13" reel



YJB100GP06H

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V, V _{GS} =0V	-	-	-1	μA
		V _{DS} =-60V, V _{GS} =0V, T _J =150°C	-	-	-100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±18V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-2.0	-2.6	-4.0	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-50A	-	6.5	8.8	mΩ
		V _{GS} =-10V, I _D =-20A	-	6.5	8.8	
		V _{GS} =-6V, I _D =-20A	-	7.2	10	
Diode Forward Voltage	V _{SD}	I _S =-50A, V _{GS} =0V	-	-0.95	-1.2	V
Gate resistance	R _G	f=1MHz, Open drain	-	9	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	-100	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-30V, V _{GS} =0V, f=1MHz	-	5370	-	pF
Output Capacitance	C _{oss}		-	970	-	
Reverse Transfer Capacitance	C _{rss}		-	72	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-30V, I _D =-20A	-	82	-	nC
Gate-Source Charge	Q _{gs}		-	25	-	
Gate-Drain Charge	Q _{gd}		-	17	-	
Reverse Recovery Charge	Q _{rr}	I _F =-20A, di/dt=500A/us	-	45	-	nC
Reverse Recovery Time	t _{rr}		-	150	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DD} =-30V, I _D =-20A R _{GEN} =1.6Ω	-	15	-	ns
Turn-on Rise Time	t _r		-	50	-	
Turn-off Delay Time	t _{D(off)}		-	135	-	
Turn-off fall Time	t _f		-	160	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T_J=25°C, V_{DD}=-50V, V_G=-10V, R_G=25Ω, L=2mH, I_{AS}=-25A.

C. P_d is based on max. junction temperature, using junction-case and junction-ambient thermal resistance.

D. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in the still air environment with T_A=25°C.

The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



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Typical Electrical and Thermal Characteristics Diagrams

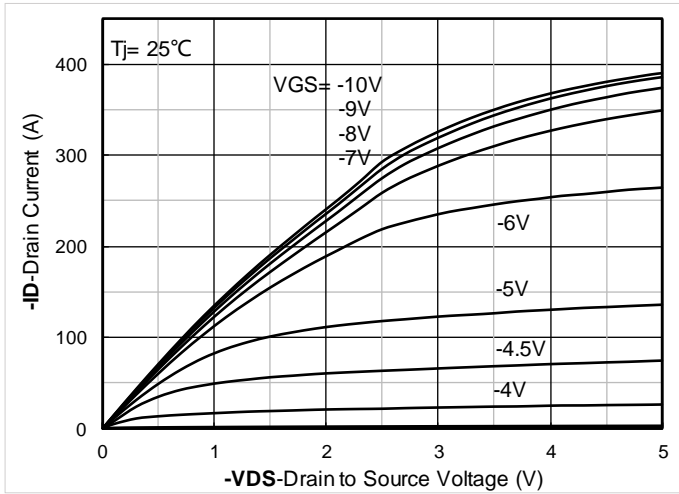


Figure 1. Output Characteristics

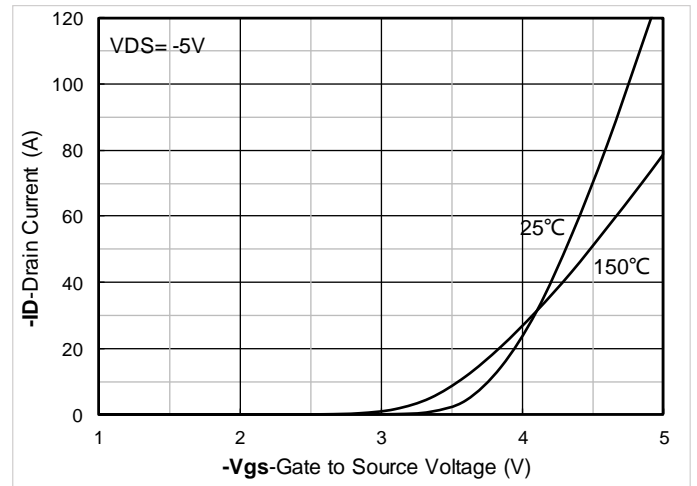


Figure 2. Transfer Characteristics

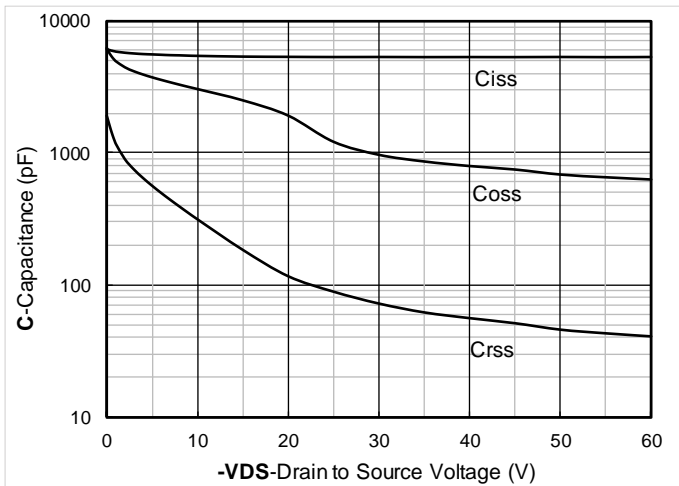


Figure 3. Capacitance Characteristics

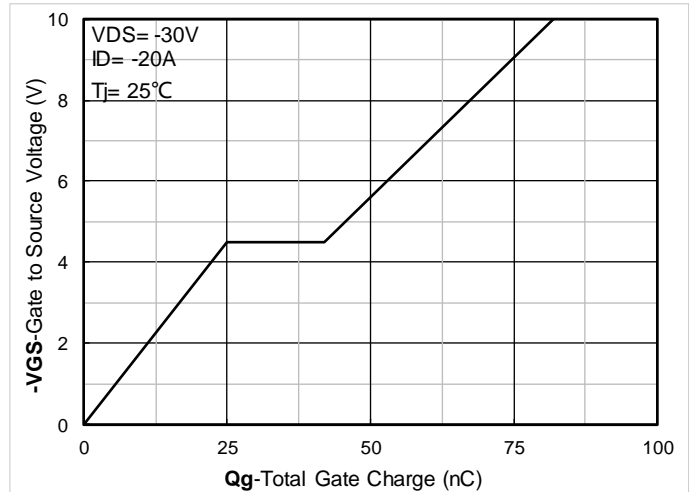


Figure 4. Gate Charge

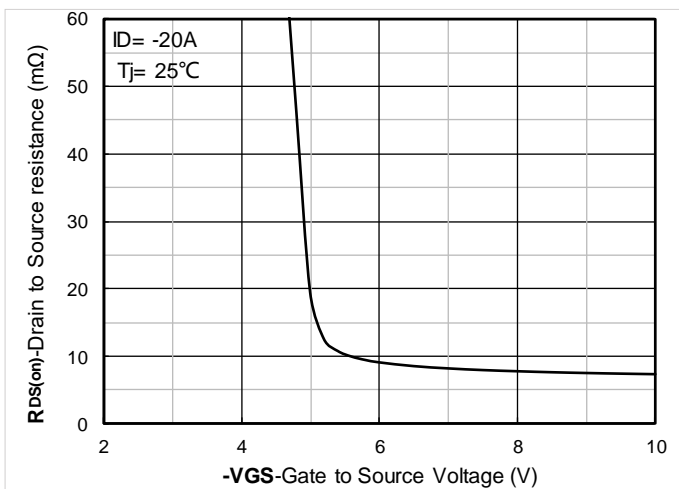


Figure 5. On-Resistance vs Gate to Source Voltage

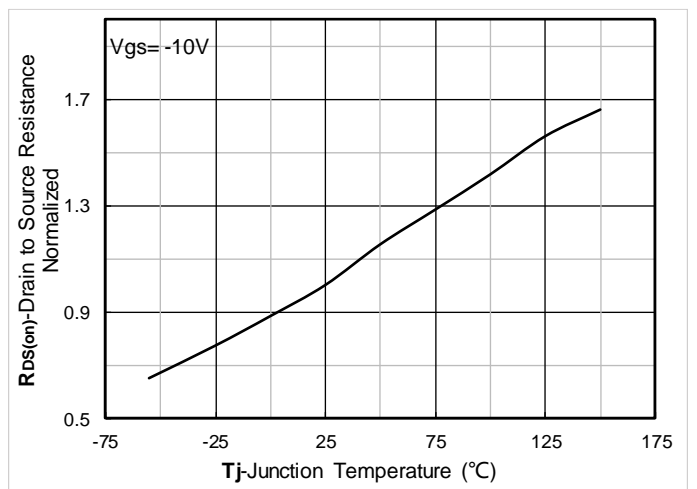


Figure 6. Normalized On-Resistance



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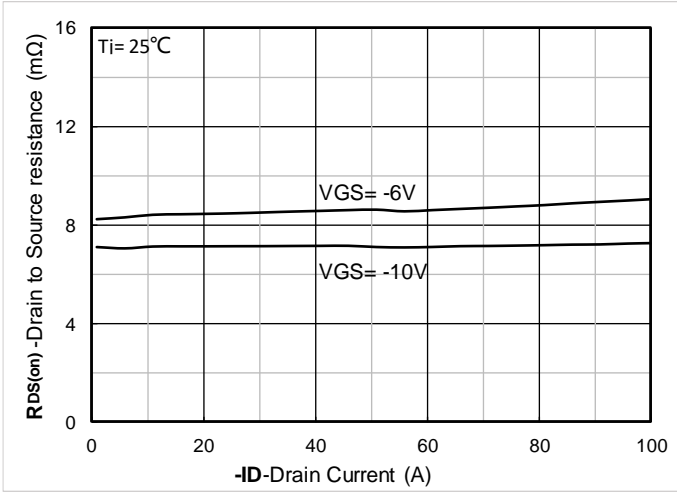


Figure 7. $R_{DS(on)}$ VS Drain Current

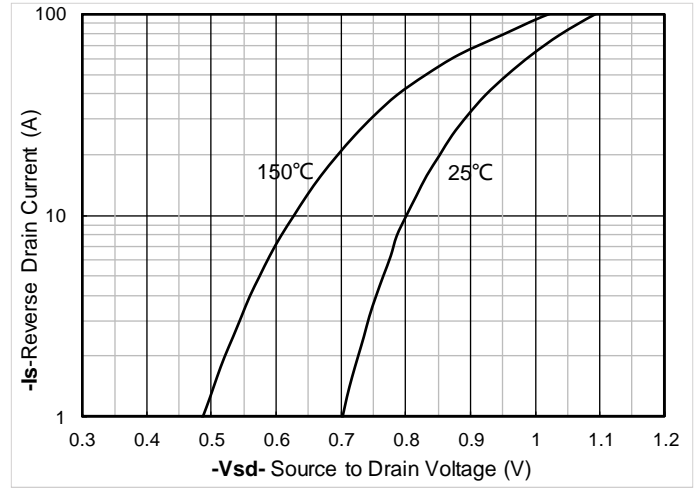


Figure 8. Forward characteristics of reverse diode

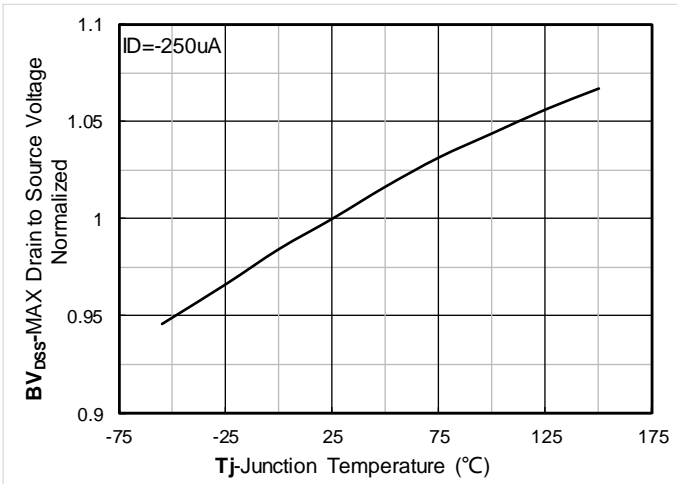


Figure 9. Normalized breakdown voltage

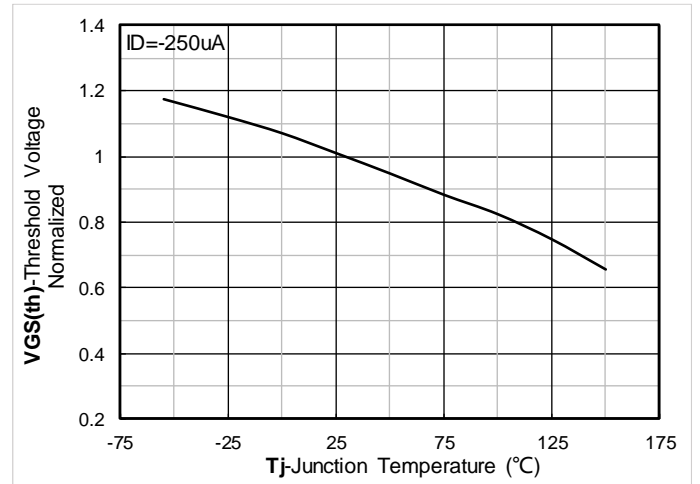


Figure 10. Normalized Threshold voltage

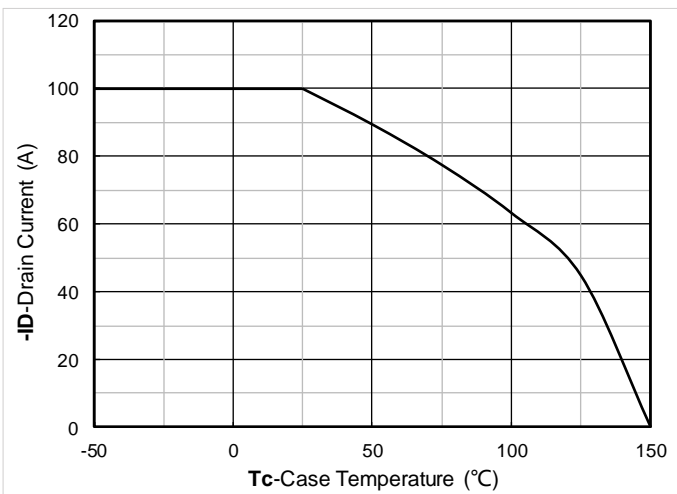


Figure 11. Current dissipation

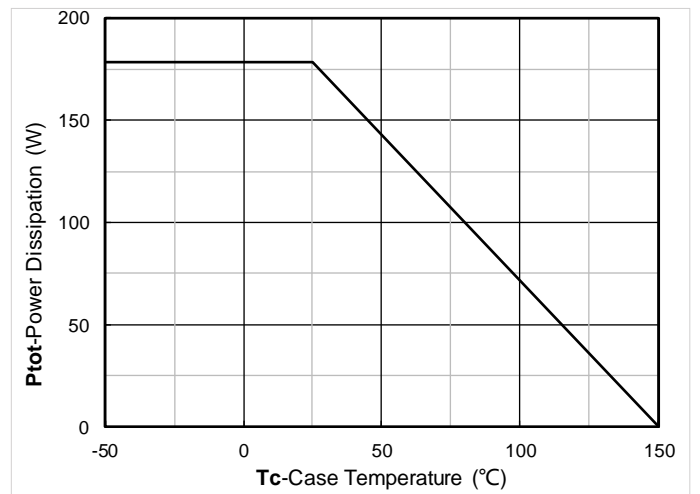


Figure 12. Power dissipation



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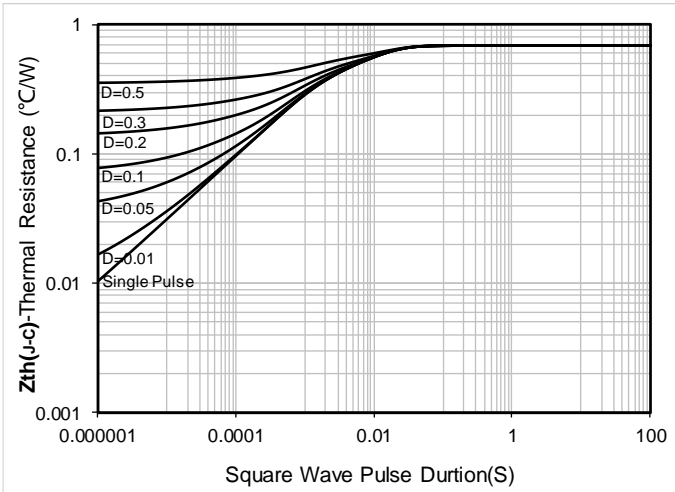


Figure 13. Maximum Transient Thermal Impedance

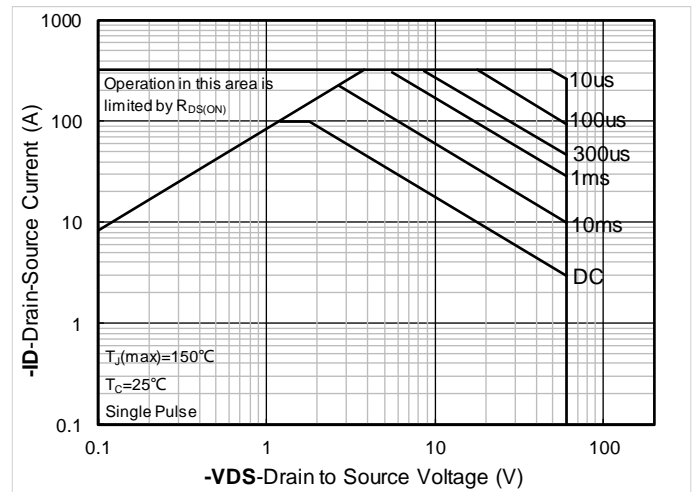
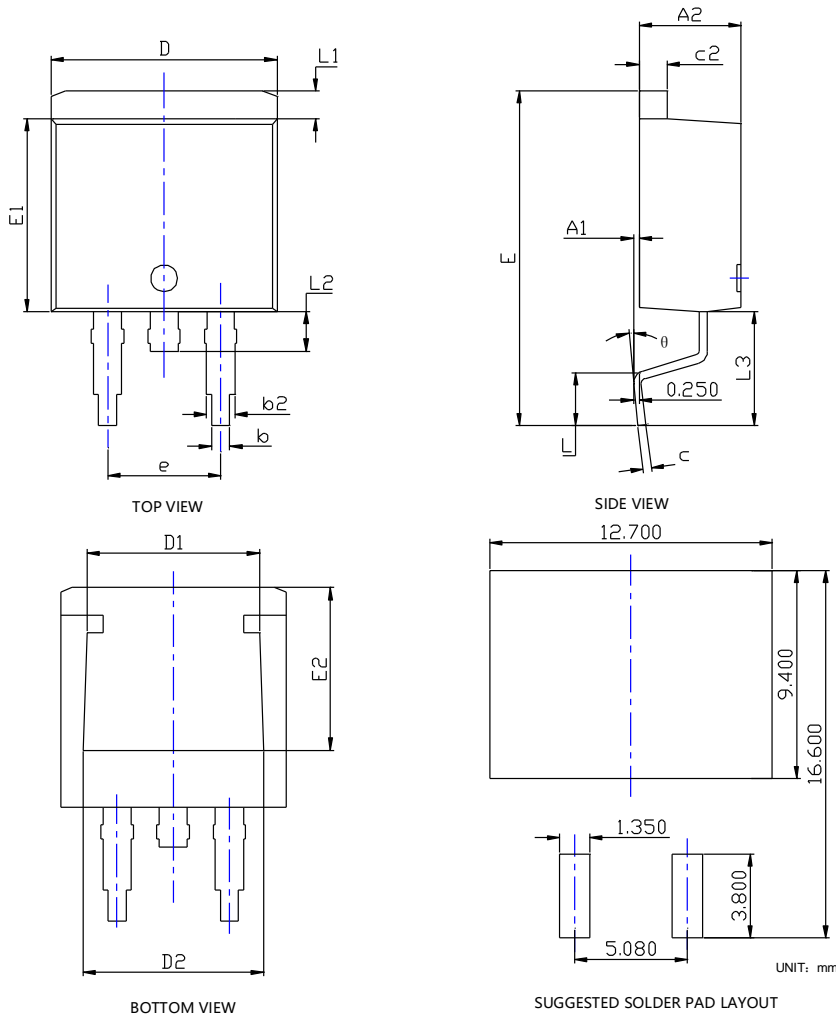


Figure 14. Safe Operation Area



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■TO-263-HY Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.
A1	0.000	---	0.010	0.000	---	0.250
A2	0.174	0.180	0.186	4.430	4.580	4.730
b	0.028	0.032	0.036	0.720	0.820	0.920
b2	0.046	0.050	0.054	1.180	1.280	1.380
c	0.013	0.015	0.018	0.330	0.390	0.450
c2	0.048	0.050	0.053	1.220	1.280	1.340
D	0.394	0.400	0.406	10.000	10.150	10.300
D1	0.295	0.307	0.319	7.500	7.800	8.100
D2	0.303	0.315	0.327	7.700	8.000	8.300
E	0.571	0.591	0.610	14.500	15.000	15.500
E1	0.337	0.341	0.348	8.550	8.700	8.850
E2	0.276	0.287	0.299	7.000	7.300	7.600
e	0.200BSC			5.080BSC		
L	0.070	---	0.110	1.790	---	2.790
L1	0.044	---	0.056	1.120	---	1.420
L2	0.030	---	0.070	0.770	---	1.770
L3	0.197REF			5.000REF		
θ	0°	---	8°	0°	---	8°

NOTE:
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



YJB100GP06H

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